PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)
	) Group Art Unit:
Suketu A. Parikh	) Examiner:
	)
Serial No.: New Divisional Application	) **PRELIMINARY AMENDMENT**
	)
Filed:	)
	) PATENT COUNSEL
For: Techniques For Triple And	) APPLIED MATERIALS, INC.
Quadruple Damascene	) Legal Affairs Department
Fabrication	) P.O. Box 450 A
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Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

PRELIMINARY AMENDMENT

This preliminary amendment is submitted for the above-identified new Divisional Patent Application, enclosed herewith, which is a division of co-pending U.S. Patent Application No. 09/165,233, filed 10/01/98. This preliminary amendment is submitted prior to a First Office Action of the division.

AMENDMENT

In the Claims:

Please withdraw claims 1-32 and 34.

Please amend the following claim as follows:

33. (once amended) A device comprising:

a) a substrate;

b) a first dielectric layer positioned on the substrate;

c) a second dielectric layer positioned on the first dielectric layer, wherein the first and second dielectric layers have dissimilar etching characteristics.

d) a third dielectric layer positioned on the second dielectric layer;

e) a fourth dielectric layer positioned on the third dielectric layer, wherein the first and fourth dielectric layers have dissimilar etching characteristics;

f) a fifth dielectric layer positioned on the fourth dielectric layer, wherein the fifth dielectric layer has dissimilar etching characteristics with regard to the second and the fourth dielectric layers, and wherein the first and fifth dielectric layers have similar etching characteristics;

g) a first region in the fifth dielectric layer defining a power line trench extending through the fifth, fourth and third dielectric layers;

h) a second region in the fifth dielectric layer defining a signal line trench extending through the fifth dielectric layer; and

i) a third region in the fourth dielectric layer underlying the signal line trench, defining a first via hole extending through the fourth, third, second and first dielectric layers, wherein the power line trench, the signal line trench and the first via hole are adapted for containing a triple damascene structure.

Please add the following new claims numbered 35-59.

35. The device of claim 33 wherein (1) the first, third and fifth dielectric layers comprise one or more dielectric materials selected from the group consisting of amorphous fluorinated carbon, organic spin-on materials, spin-on-glass, aero-gel, poly(arylene)ethers, fluorinated poly(arylene)ethers and divinyl siloxane benzo-cyclobutane and (2) the second and fourth dielectric layers comprise one or more dielectric materials selected from the group consisting of SiO_2 and fluorinated SiO_2.

36. The device of claim 33 wherein (1) the first, third and fifth dielectric layers comprise one or more dielectric materials selected from the group consisting of SiO_2 and fluorinated SiO_2 and (2) the second and fourth dielectric layers comprise one or more dielectric materials selected from the group consisting of amorphous fluorinated carbon, organic spin-on materials, spin-on-glass, aero-gel, poly(arylene)ethers, fluorinated poly(arylene)ethers and divinyl siloxane benzocyclobutane.

37. The device of claim 33 additionally comprising a conductive material positioned in the power line trench, the signal line trench and the first via hole, thereby forming a power line, a signal line and a first via plug.

38. The device of claim 37 wherein the power line comprises a substantially greater thickness than the signal line.

39. The device of claim 33 additionally comprising a fourth region in the second dielectric layer underlying the power line trench, defining a second via hole extending through the second and first dielectric layers, wherein the power line trench, the signal trench, the first via hole and the second via hole are adapted for containing a quadruple damascene structure.

40. The device of claim 39 additionally comprising a conductive material positioned in the power line trench, the signal trench, the first via hole and the second via hole.

41. A device comprising:

a) a substrate;

b) a cap layer positioned on the substrate;

c) a first dielectric layer positioned on the cap layer;

d) a second dielectric layer positioned on the first dielectric layer, wherein the first and second dielectric layers have dissimilar etching characteristics;

e) a third dielectric layer positioned on the second dielectric layer;

f) a fourth dielectric layer positioned on the third dielectric layer, wherein (1) the first and fourth dielectric layers have dissimilar etching characteristics and (2) the cap layer and the second and fourth dielectric layers have similar etching characteristics;

g) a fifth dielectric layer positioned on the fourth dielectric layer, wherein (1) the fifth dielectric layer has dissimilar etching characteristics with regard to the

cap layer and the second and fourth dielectric layers and (2) the first and fifth dielectric layers have similar etching characteristics;

h) a first region in the fifth dielectric layer defining a power line trench extending through the fifth, fourth, third and second dielectric layers;

i) a second region in the fifth dielectric layer defining a signal line trench extending through the fifth and fourth dielectric layers; and

j) a third region in the third dielectric layer and underlying the signal trench line, defining a first via hole extending from the third dielectric layer to the substrate, wherein the power line trench, the signal line trench and the first via hole are adapted for containing a triple damascene structure.

42. The device of claim 41 additionally comprising a conductive material positioned in the power line trench, the signal line trench and the first via hole, thereby forming a power line, a signal line and a first via plug.

43. The device of claim 42 wherein the power line comprises a substantially greater thickness than the signal line.

44. The device of claim 41 additionally comprising a fourth region in the first dielectric layer and underlying the power line trench, defining a second via hole extending from the power line trench to the substrate, wherein the power line trench, the signal line trench, the first via hole and the second via hole are adapted for containing a quadruple damascene structure.

45. The device of claim 44 additionally comprising a conductive material positioned in the power line trench, the signal line trench, the first via hole and the second via hole.

46. A device comprising:

a) a substrate;

b) a first dielectric layer positioned on the substrate;

c) a second dielectric layer positioned on the first dielectric layer, wherein the first and second dielectric layers have dissimilar etching characteristics;

d) a third dielectric layer positioned on the second dielectric layer, wherein (1) the second and third dielectric layers have dissimilar etching characteristics and (2) the first and third dielectric layers have similar etching characteristics;

e) a first region in the third dielectric layer defining a power line trench extending through the third and second dielectric layers;

f) a second region in the third dielectric layer defining a signal line trench extending to the first dielectric layer; and

g) a third region in the first dielectric layer and underlying the signal trench, defining a first via hole extending from the signal line trench to the substrate.

47. The device of claim 46 additionally comprising a conductive material positioned in the power line trench, the signal line trench and the first via hole, thereby forming a power line, a signal line and a first via plug.

48. The device of claim 47 wherein the power line comprises a substantially greater thickness than the signal line.

49. The device of claim 46 additionally comprising a fourth region in the first dielectric layer and underlying the power line trench defining a via hole extending from the power line trench to the substrate.

50. The device of claim 49 additionally comprising a conductive material positioned in the power line trench, the signal line trench, the first via hole and the second via hole.

51. A device comprising:

a) a substrate;

b) a first dielectric layer positioned on the substrate;

c) a second dielectric layer positioned on the first dielectric layer;

d) a third dielectric layer positioned on the second dielectric layer, wherein the first, second and third dielectric layers have similar etching characteristics;
e) a first region in the third dielectric layer defining a power line trench extending through the third and second dielectric layers;
f) a second region in the third dielectric layer defining a signal line trench extending through the third dielectric layer; and
g) a third region in the second dielectric layer and underlying the signal line trench, defining a first via hole extending from the signal line trench to the substrate.

52. The device of claim 51 additionally comprising a conductive material positioned in the power line trench, the signal line trench and the first via hole, thereby forming a power line, a signal line and a first via plug.

53. The device of claim 52 wherein the power line comprises a substantially greater thickness than the signal line.

54. The device of claim 51 additionally comprising a fourth region in the first dielectric layer and underlying the power line trench, defining a second via hole extending from the power line trench to the substrate.

55. The device of claim 54 additionally comprising a conductive material positioned in the power line trench, the signal line trench, the first via hole and the second via hole.

56. An integrated circuit structure fabricated in accordance with a process comprising:
a) depositing a first dielectric layer on a substrate;
b) depositing a second dielectric layer on the first dielectric layer, wherein the first and second dielectric layers have dissimilar etching characteristics;
c) depositing a third dielectric layer on the second dielectric layer;

d) depositing a fourth dielectric layer on the third dielectric layer, wherein the first and fourth dielectric layers have dissimilar etching characteristics;

e) depositing a fifth dielectric layer on the fourth dielectric layer, wherein the fifth dielectric layer has dissimilar etching characteristics with regard to the second and the fourth dielectric layers, and wherein the first and fifth dielectric layers have similar etching characteristics;

f) simultaneously anisotropically etching a power line trench and a via pattern through the fifth, fourth and third dielectric layers, in a first etching sequence; and

g) anisotropically etching a signal line trench, overlaying the via pattern, through the fifth dielectric layer, and anisotropically etching the via pattern to the substrate thereby forming a via hole extending from the signal line trench to the substrate, in a second etching sequence, wherein a integrated circuit structure is fabricated including the power line trench and the signal trench having an underlying via hole.

57. An integrated circuit structure fabricated in accordance with a process comprising:

a) depositing a cap layer on a substrate;

b) depositing a first dielectric layer on the cap layer;

c) depositing a second dielectric layer on the first dielectric layer, wherein the first and second dielectric layers have dissimilar etching characteristics;

d) depositing a third dielectric layer on the second dielectric layer;

e) depositing a fourth dielectric layer on the third dielectric layer, wherein the first and fourth dielectric layers have dissimilar etching characteristics, and wherein the cap layer and the second and fourth dielectric layers have similar etching characteristics;

f) depositing a fifth dielectric layer on the fourth dielectric layer, wherein the fifth dielectric layer has dissimilar etching characteristics with regard to the cap layer and to the second and the fourth dielectric layers, and wherein the first and fifth dielectric layers have similar etching characteristics;

g) simultaneously anisotropically etching a power line trench pattern and a via pattern through the fifth, fourth and third dielectric layers, in a first etching sequence; and

h) anisotropically etching a signal line trench, overlaying the via pattern, through the fifth and fourth dielectric layers, anisotropically etching the via pattern to the substrate thereby forming a via hole e4xtending from the signal line trench to the substrate, and anisotropically etching the power line trench pattern through the second dielectric layer thereby forming a power line trench, in a second etching sequence.

58. An integrated circuit structure fabricated in accordance with a process comprising:

a) depositing a first dielectric layer on a substrate;

b) depositing a second dielectric layer on the first dielectric layer, wherein the first and second dielectric layers have dissimilar etching characteristics;

c) depositing a third dielectric layer on the second dielectric layer, wherein the second and third dielectric layers have dissimilar etching characteristics and wherein the first and third dielectric layers have similar etching characteristics;

d) simultaneously anisotropically etching a power line trench and a via pattern through the third and second dielectric layers, in a first etching sequence; and

e) anisotropically etching a signal line trench, overlaying the via pattern, through the third dielectric layer, and simultaneously etching the via pattern to the substrate thereby forming a via hole extending from the signal line trench to the substrate, in a second etching sequence.

59. An integrated circuit structure fabricated in accordance with a process comprising:

a) depositing a first dielectric layer on a substrate;

b) depositing a second dielectric layer on the first dielectric layer;

c) depositing a third dielectric layer on the second dielectric layer, wherein the first, second and third dielectric layers have similar etching characteristics;

d) simultaneously anisotropically etching a power line trench pattern and a via pattern through the third and second dielectric layers, in a first etching sequence; and

e) anisotropically etching a signal line trench, overlaying the via pattern, through the third dielectric layer, and simultaneously anisotropically etching the via pattern to the substrate thereby forming a via hole extending from the signal line trench to the substrate, in a second etching sequence.

REMARKS

Claim 33 of the original co-pending parent application as filed has been amended. Claims 1-32 and 34 of the parent application as filed are withdrawn because these claims are drawn to an invention that is non-elected in the present divisional application. New claims 35-59 have been added.

I. Once amended claim 33

Claim 33 has been amended inserting the term "first" before "via hole" (clause i) because applicant recites a "second via hole" in new independent claim 38.

II. New Claims

Support for new claims 35-59 is found in claim 33 of the parent application as filed, and in the specification and drawing of the parent application as filed.

In view of the above, applicant hereby respectfully request examination of the application, including amended claim 33 and new claims 35-59.

Respectfully submitted,

Dated: April 25, 2001

By: ______________________
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